## REMARKS

Claims 57-59, 66 and 72-75 are amended. Claims 76 and 77 are cancelled. Claims 82-92 are added. Claims 57-75 and 78-92 are in the application for consideration.

Applicant appreciates the Examiner's indicated allowability of the subject matter of claims 58 and 59.

Claim 57 is amended to recite that the conductive diffusion barrier layer comprises at least two $W_xN_y$, $TiO_xN_y$ and $TiW_xN_y$. Claim 57 is believed to be allowable for analogous reasons under which the Examiner found claims 58 and 59 allowable. Claims 58 and 59 have been amended to retain the originally allowed subject. For at least the foregoing reasons, Applicant's claims 57-61 should be formally allowed, and action to that end is requested.

Independent claim 62 stands rejected as being obvious over a combination of Pfiester in view of Wu and either Hachiya or Dennison. Applicant disagrees and requests reconsideration.

Pfiester does not in any way disclose a contact structure to a gate, as its gate is shown as having a conductive region defined by conductive layers 16, 30 and 20, the sides and tops thereof which are everywhere covered by an insulating layer 44. Accordingly, none of regions 38, 36 or 40 of the illustrated P+ poly is in electrical connection with its above-defined gate. Apparently, Wu is relied upon for its conductive contact 24b making electrical connection with its gate stack 18a/16c/16b/16a. However, Wu clearly only discloses that its material 24b is formed of tungsten, or of conductively doped polysilicon but does not disclose conductivity type. Further, the Examiner erroneously asserts on page 6 of the Office Action that Wu teaches "such that the conductive diffusion barrier layer of the gate being provided between the gate semiconductive material

provided through the insulative material". However, Wu in no way discloses or suggests a conductive diffusion barrier layer effective to restrict the diffusion of first or second conductivity-enhancing impurity in its gate construction.

The Examiner's reliance upon Hachiya or Dennison in the obviousness rejection is not understood, nor seen to add anything beyond the Wu teaching. Specifically, it is acknowledged that Wu teaches a contact structure through insulative material, albeit metal, whereas each of Hachiya and Dennison teach a contact structure through insulative material of different conductivity types at different locations on the substrate. However, each of Hachiya and Dennison are seen to disclose such contact structures where P+ material is in contact with a P+ region, and N+ material is in contact with an N+ region, and therefore teaches away from claim 62. There is no teaching or suggestion in either Hachiya or Dennison of having a contact structure of a first conductivity type in electrical contact with a region of second conductivity type, or vice versa, in making electrical contact within integrated circuitry to anything, let alone to a transistor.

The undersigned acknowledges that Pfiester clearly discloses a gate structure having first and second conductivity type conductive semiconductive material regions having a diffusion barrier layer sandwiched therebetween. However, Applicant's independent claim 62 is clearly directed to the combination of a contact structure and a field effect transistor gate. Required in the combination is that the gate have conductively doped semiconductive material of one type and the contact structure have conductively doped semiconductive material of another type. Not one of the relied upon references teaches making electrical connection with a contact structure of one conductivity type to a field effect transistor having material of another conductivity type. Pfeister is only

material to the concept of having a gate construction having two different conductivity types therein, and is not material to any contact structure making electrical contact with the transistor gate. The reference does not teach, nor would it be obvious to a person of skill in the art to utilize any of the conductive materials of the transistor gate within a separate contact structure to that gate. Wu teaches a metal contact or conductively doped polysilicon to a silicide layer of a polysilicon/silicide gate, but nothing is said about the conductivity type of the poly. The relied upon Hachiya and Dennison references only disclose making electrical connection between same conductivity type materials. The collective teaching of the combined references is to make electrical connection between same conductive type materials with metal or with material of the same conductivity type, not what Applicant recites in claim 62.

Not one of the references teaches a contact structure making electrical connection to a transistor gate wherein the contact structure and transistor gate themselves comprise semiconductive material respectively conductively doped with opposite type conductivity enhancers. As each of the references is lacking in any way of making electrical connection of a contact structure to any other device where the contact structure and device are of opposite conductivity types, the references clearly could in no way suggest doing so in the manner specifically claimed by Applicant regarding the utilization of the recited diffusion barrier material.

For at least the foregoing reasons, Applicant's independent claim 62 as currently presented is seen to be allowable over the applied references. Formal allowance is therefore urged.

Applicant's previously submitted dependent claims should be allowed as depending from allowable base claims, and for their own recited features which

are neither shown nor suggested in the cited art. Specifically, and by way of example only with respect to claim 67, such recites that the semiconductive material of the contact structure contacts the conductive diffusion barrier layer of the gate. None of Wu, Hachiya or Dennison disclose a conductive diffusion barrier layer, and accordingly, in no way disclose or suggest making the contact in the way Applicant recites in claim 67. Regarding Pfeister, it does not even disclose forming an electrical contact to its gate, and accordingly, could in no way suggest physically contacting the conductive diffusion barrier layer. Even if, by some stretch of the imagination, a contact structure were conceived in conjunction with the Fig. 7 construction of Pfeister, such would clearly only contact the upper surface of layer 20, and not conductive diffusion barrier layer 30. For at least these additional reasons, dependent claim 67 should be allowed, and action to that end is requested.

Dependent claims 82-91 are added. Claims 82-84, 86-88 and 90-92 are patterned analogously to allowable claims 57-59. Accordingly, such claims should summarily be allowed, both as depending from allowable base claims and at least for other reasons for which claims 57-59 are allowable. Added dependent claims 85 and 86 add to the claim 62 combination that the gate to which the contact structure is making connection is defined by a single conductive region. In claim 85, that single conductive region is stated to consist of conductively doped semiconductive material of the first type and the conductive diffusion barrier layer. In claim 89, that single conductive region is stated to consist of the conductively doped semiconductive material of the first type, the conductive diffusion barrier layer, and a silicide. Support for the same can be found in Applicant's application as-filed in the paragraph spanning pages 7 and 8. Accordingly, no new matter is added thereby. Claims 85 and 89 should be

allowed as depending from an allowable base claim, and for their own recited features which are neither shown nor suggested in the cited art. For example, Pfeister clearly discloses utilizing semiconductive material of multiple conductivity types in its transistor, and accordingly, specifically teaches away from a gate defined by a single conductive region that consists of the stated elements of claims 85 and 89, respectively. Therefore, allowance of these claim is urged on their own merits.

This application is believed to be in immediate condition for allowance, and action to that end is requested.

Respectfully submitted,

Dated: 9-3-02

By: _____
Mark S. Matkin
Reg. No. 32,268

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application Serial No. ..... 09/730,335
Filing Date ..... December 4, 2000
Inventor ..... Charles H. Dennison
Assignee ..... Micron Technology, Inc.
Group Art Unit ..... 2811
Examiner ..... Ori Nadav
Attorney's Docket No. ..... MI22-1577
Title: Field Effect Transistors and Integrated Circuitry

## VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO JUNE 4, 2002 FINAL OFFICE ACTION

**In the Claims**



The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

57. (Twice Amended) A field effect transistor comprising:

a pair of source/drain regions having a channel region positioned therebetween; and

a gate positioned operatively proximate the channel region, the gate comprising semiconductive material conductively doped with at least one of a p-type or n-type conductivity enhancing impurity effective to render the semiconductive material electrically conductive, a silicide layer and a conductive diffusion barrier layer effective to restrict diffusion of p-type or n-type conductivity enhancing impurity, the conductive diffusion barrier layer comprising at least two of $W_xN_y$, $TiO_xN_y$ and $TiW_xN_y$.

58. (Amended) The transistor of claim 57 wherein the conductive diffusion barrier layer comprises $W_xN_y$ and $TiW_xN_y$.

59. (Amended) The transistor of claim 57 wherein the conductive diffusion barrier layer comprises $TiO_xN_y$ and $TiW_xN_y$.

66. (Amended) The ~~transistor~~ integrated circuitry of claim 65 wherein the silicide and the conductive diffusion barrier layer comprise the same metal.

72. (Twice Amended) The ~~transistor~~ integrated circuitry of claim 62 wherein the conductive diffusion barrier layer comprises a material selected from the group consisting of $W_xN_y$, $TiO_xN_y$, and $TiW_xN_y$, and mixtures thereof.

73. (Amended) The ~~transistor~~ integrated circuitry of claim 72 wherein the conductive diffusion barrier layer comprises $W_xN_y$.

74. (Amended) The ~~transistor~~ integrated circuitry of claim 72 wherein the conductive diffusion barrier layer comprises $TiO_xN_y$.

75. (Amended) The ~~transistor~~ integrated circuitry of claim 72 wherein the conductive diffusion barrier layer comprises $TiW_xN_y$.

Claims 76 and 77 are cancelled.

New claims 82-92 are added.

**END OF DOCUMENT**